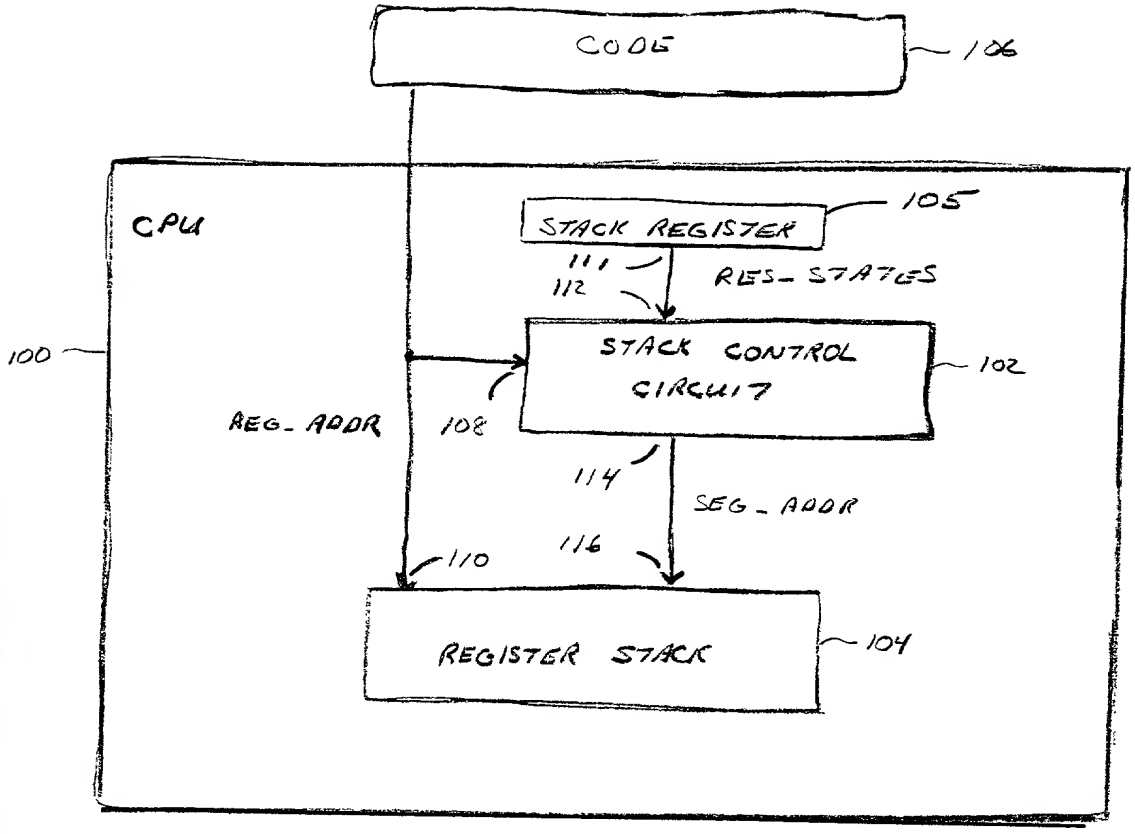
CODE
106
CPU
STACK REGISTER
105
111
112
RES_STATES
100
STACK CONTROL CIRCUIT
102
REG_ADDR
108
114
SEG_ADDR
110
116
REGISTER STACK
104

FIG. 1

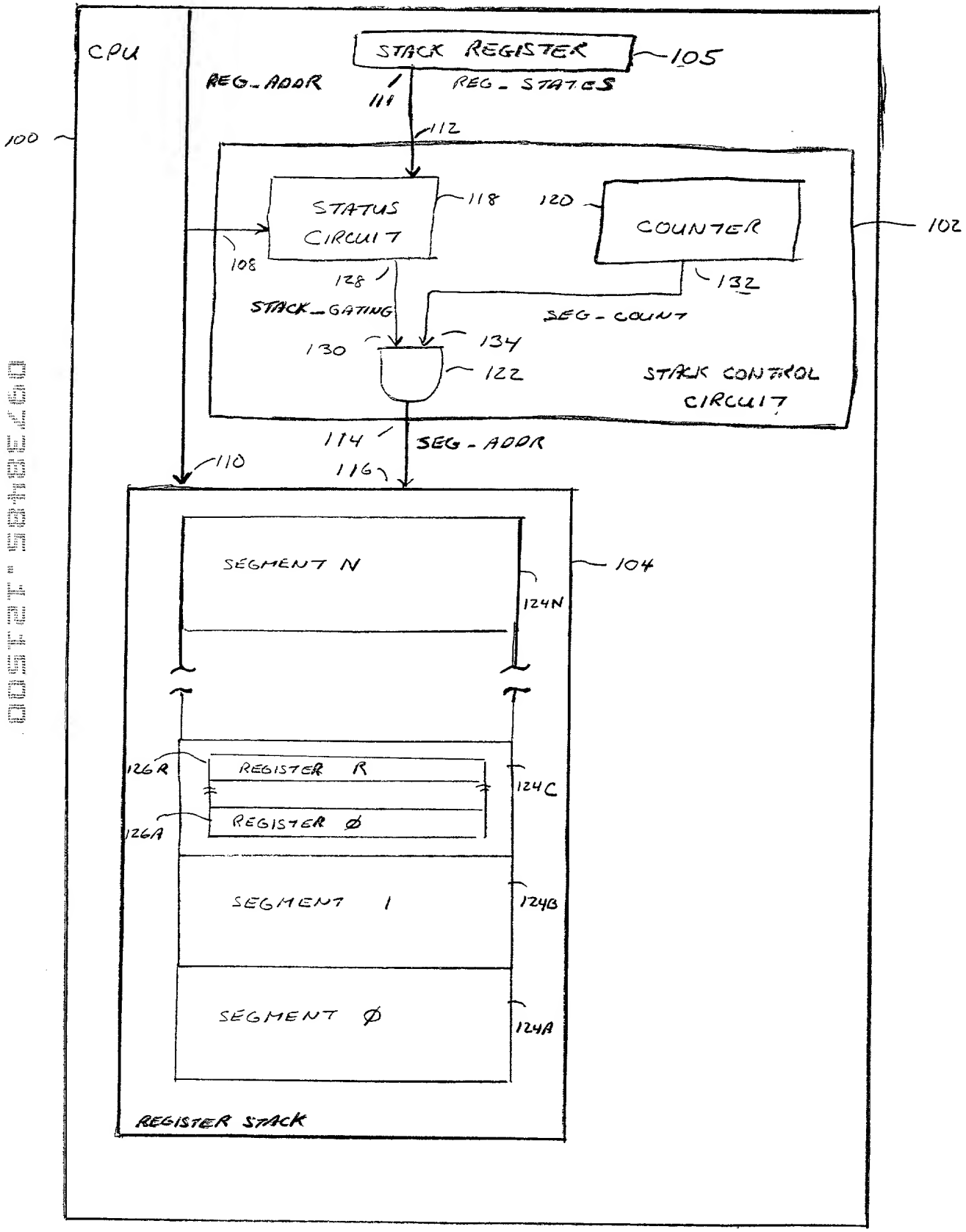
CPU
100
STACK REGISTER
105
REG_ADDR
111
REG_STATES
112
STATUS CIRCUIT
118
120
COUNTER
102
108
128
132
STACK_GATING
SEG_COUNT
130
134
122
STACK CONTROL CIRCUIT
114
SEG_ADDR
116
110
SEGMENT N
104
124N
126R
REGISTER R
124C
126A
REGISTER Ø
SEGMENT 1
124B
SEGMENT Ø
124A
REGISTER STACK

FIG 2

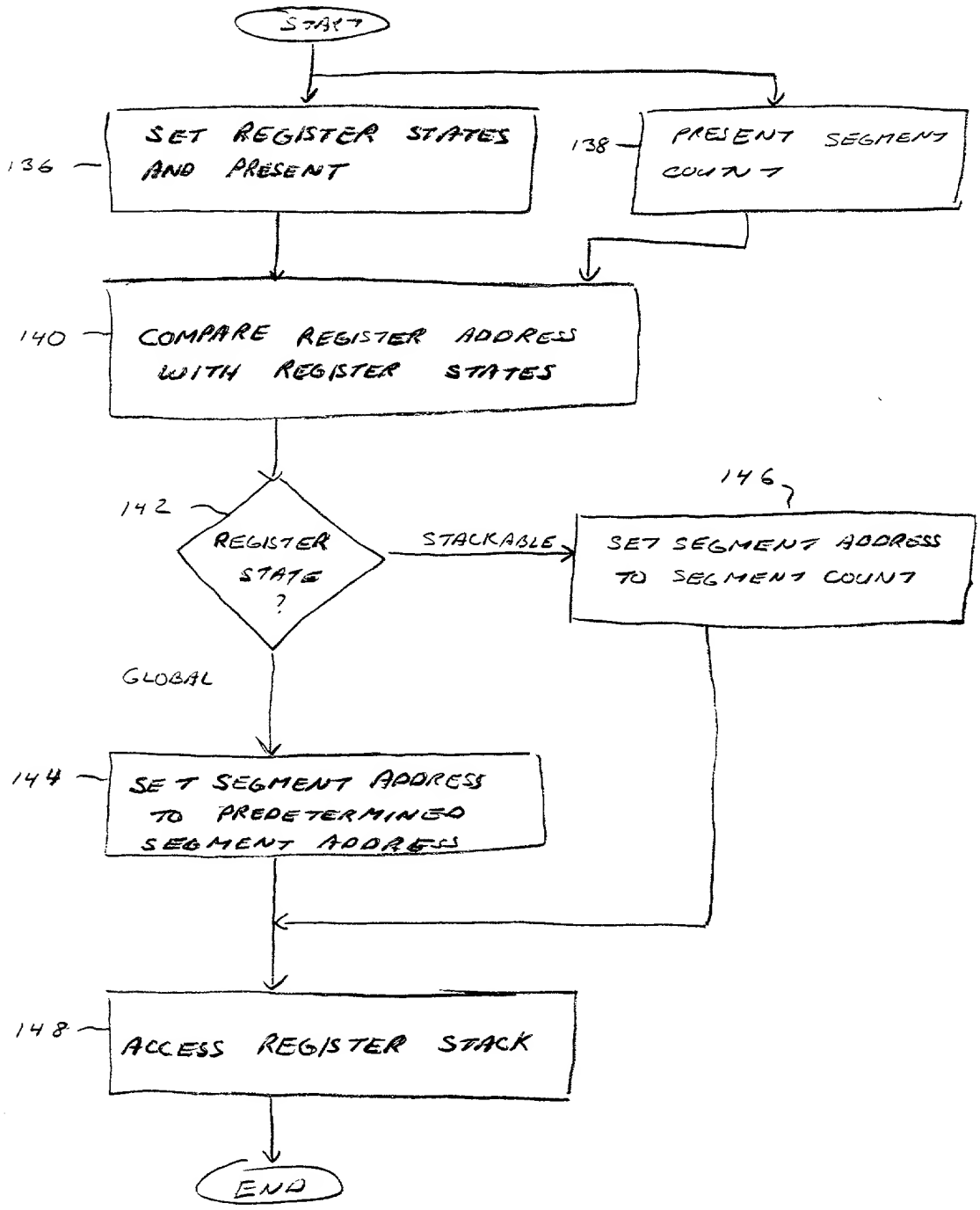
START
SET REGISTER STATES AND PRESENT
136
PRESENT SEGMENT COUNT
138
COMPARE REGISTER ADDRESS WITH REGISTER STATES
140
142
REGISTER STATE ?
STACKABLE
146
SET SEGMENT ADDRESS TO SEGMENT COUNT
GLOBAL
144
SET SEGMENT ADDRESS TO PREDETERMINED SEGMENT ADDRESS
148
ACCESS REGISTER STACK
END

FIG. 3

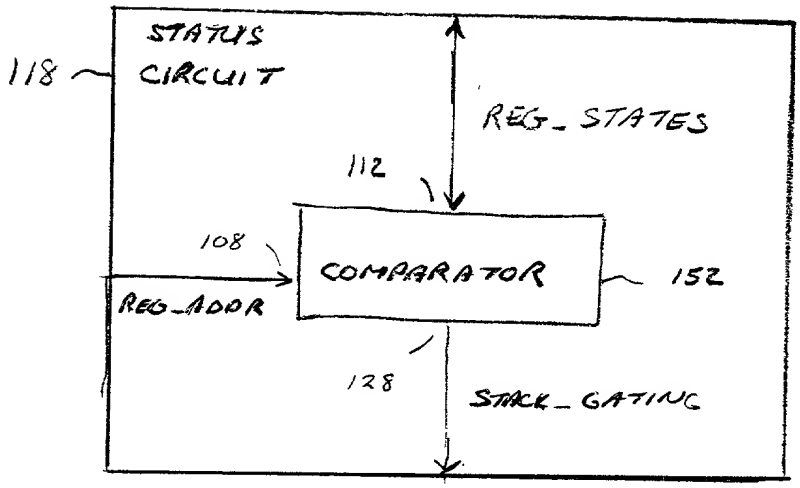
STATUS
CIRCUIT
118
REG_STATES
112
108
COMPARATOR
152
REG_ADDR
128
STACK_GATING

FIG. 4

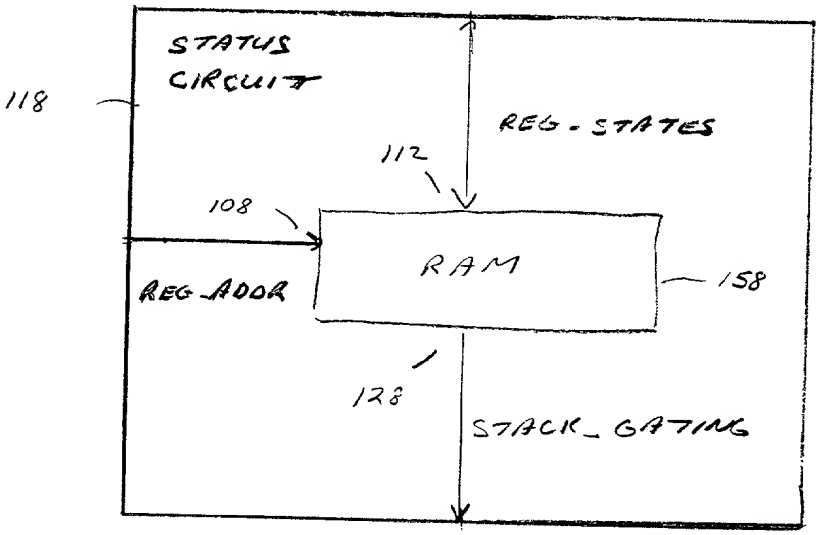
STATUS
CIRCUIT
118
REG-STATES
112
108
RAM
158
REG_ADDR
128
STACK_GATING

FIG. 5

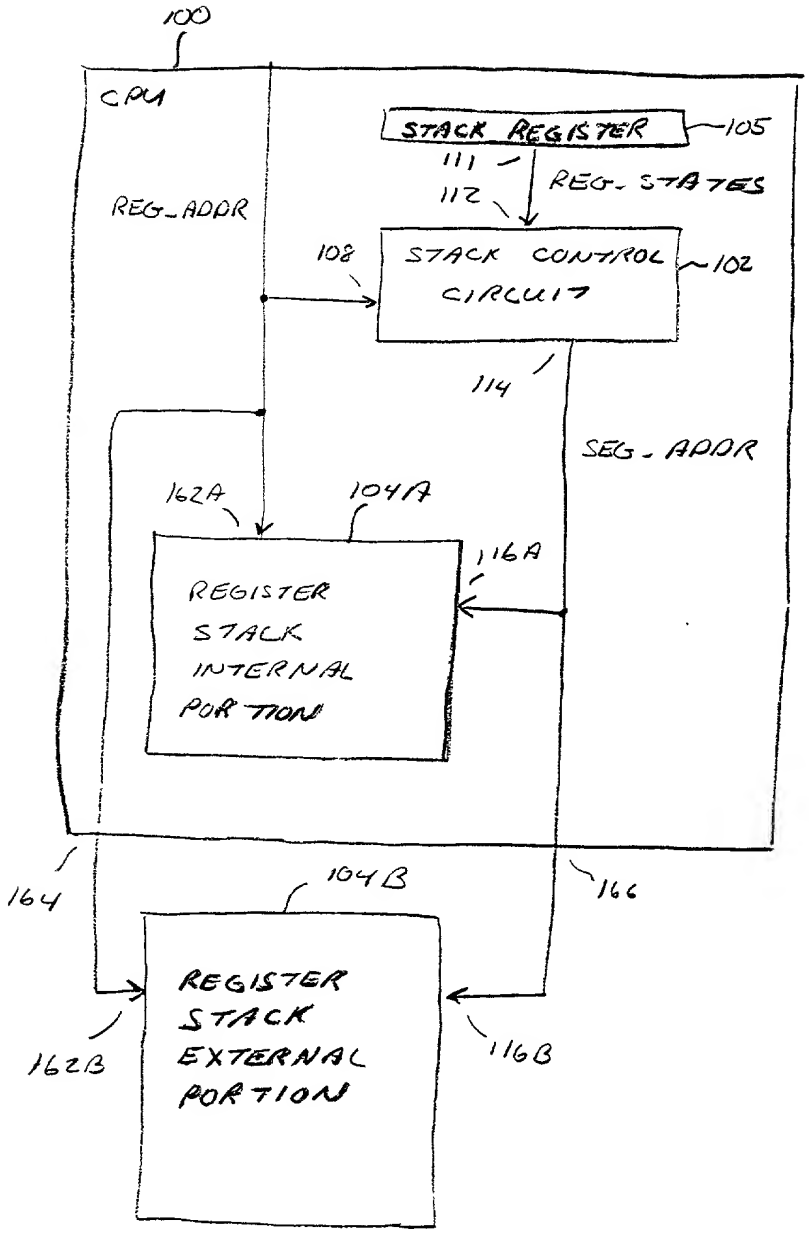
100
CPU
STACK REGISTER
105
111
112
REG. STATES
REG_ADDR
108
STACK CONTROL CIRCUIT
102
114
SEG. ADDR
162A
104A
116A
REGISTER STACK INTERNAL PORTION
164
104B
166
REGISTER STACK EXTERNAL PORTION
162B
116B

FIG. 6

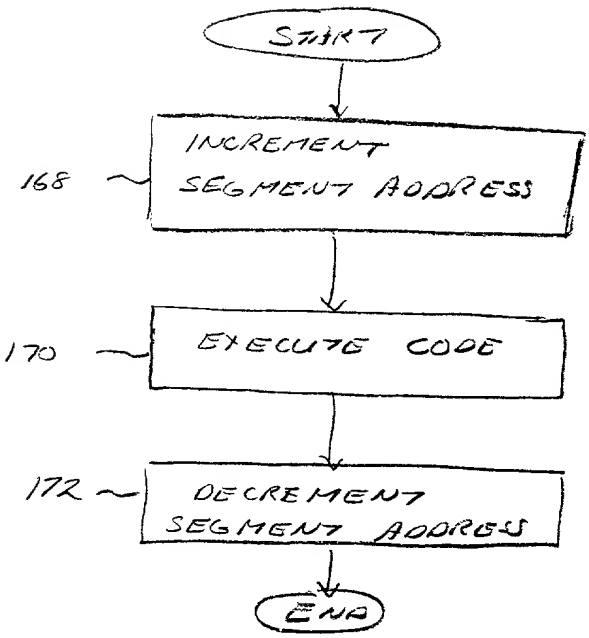
START
INCREMENT SEGMENT ADDRESS
168
EXECUTE CODE
170
DECREMENT SEGMENT ADDRESS
172
END

FIG. 7